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EXAMINER	
AHMED, SALMAN	
ART UNIT	**PAPER NUMBER**
2616	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/722,727	NARAD, CHARLES E.	
	Examiner	Art Unit	
	Salman Ahmed	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/25/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/25/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-28 are pending.

Claims 1-28 are rejected.

Specification

1. The disclosure is objected to because of the following informalities: Page 4 line 10 of the Specification the word "cull" should be changed to –pull--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5, 8-11, 13, 14, 16, 17, 19-23 and 25-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang (US PAT PUB 2003/0210652) in view of Raphaeli et al. (US PAT PUB 2003/0103521, hereinafter Raphaeli).

In regards to claims 1 and 25 Chiang teaches *a set of at least one component to Handle packets, comprising: a first component* (Figure 2, MAC 621), *comprising: an input interface to receive data of packets* (Figure 2, physical layer device (PHY) 622); *an output interface* (Figure 2, a direct memory access (DMA) engine 6214); *circuitry* (Figure 2, control packet generator 6212) *to: generate packets such that data values*

within the generated packet payloads include data originating within the first component (section 0030, depending on the types of objects, various management information data are included in the control packet CP, for example the number of received packets, number of transmitted data, colliding packets, CRC error, over-sized packets, under-sized packets, packet settings, packet parameters and/or specially defined packet particulars); *and transmit packets via the output interface* (Figure 2, transmitting via direct memory access (DMA) engine 6214) *to a component* (layer 75) *further along a receive path monotonically ascending layers of a protocol stack* (section 0035, The third to seventh layers, indicated by a numeral reference 75, are equivalent to upper-level application programs, e.g. the network communication protocol, the SNMP and other communication protocol layers), *the packets to transmit including the generated packets* (control packets CP) *and packets including data of packets* (data packets DP) *received via the input interface* (section 0035, In a receiving procedure, the control packet CP is generated in the layer 72 and then put into the data packets DP to be transmitted to the layer 74. The data packets DP and the control packet CP are then respectively transmitted to the layer 75 via the layer 74).

Chiang does not explicitly teach control packet having a header with payload as in claim 1. Chiang does not explicitly teach having a header for identification by component further along the receive path, as in claim 25.

Raphaeli in the same field of endeavor teaches control packets having a header with payload (section 0265-0267, the frame format for the control frame is comprised of a frame control (header) followed by a payload).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang's system/method by incorporating the control packets having header portion and payload portion as suggested by Raphaeli. The motivation is that, (as suggested by Raphaeli, section 0271) the frame header provides parameters about the frame payload and enables a system to efficiently and reliably identify the frame type (control frame, data frame, status frame etc.) and related frame parameters.

In regards to claim 28, Chiang teaches *a method, the method comprising: generating, at a first component* (Figure 2, MAC 621), *a packet having a payload including data originating within the first component* (section 0030, depending on the types of objects, various management information data (*payload*) are included in the generated control packet CP, for example the number of received packets, number of transmitted data, colliding packets, CRC error, over-sized packets, under-sized packets, packet settings, packet parameters and/or specially defined packet particulars); *and transmitting the packet to a second component* (layer 75) *further along a receive path monotonically ascending layers of a protocol stack* (section 0035, In a receiving procedure, the control packet CP is generated in the layer 72 and then put into the data packets DP to be transmitted to the layer 74. The data packets DP and the control packet CP are then respectively transmitted to the layer 75 via the layer 74).

Chiang does not explicitly teach packet having a header with payload.

Raphaeli in the same field of endeavor teaches packets having a header with payload (section 0265-0267, the frame format for the control frame is comprised of a frame control (header) followed by a payload).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang's system/method by incorporating the packets having header portion and payload portion as suggested by Raphaeli. The motivation is that, (as suggested by Raphaeli, section 0271) the frame header provides parameters about the frame payload and enables a system to efficiently and reliably identify the frame type (control frame, data frame, status frame etc.) and related frame parameters.

In regards to claim 2, Chiang teaches *first component* (Figure 2, MAC 621) *comprises a PHY* (Figure 2, physical layer device (PHY) 622).

In regards to claim 3, Chiang teaches *the input interface comprises signal to digital conversion circuitry, the circuitry operating on at least one of the following: optic signals, wire signals* (section 0009 Ethernet network), *and wireless signals* (section 0003, the physical layer device 12 receives and converts (digital conversion circuitry) packets from the network (section 0009 Ethernet network) into desired forms, such as digital forms).

In regards to claim 5, Chiang teaches *the data originating within the first component comprises at least one status of the PHY* (section 0030, depending on the types of objects, various management information data are included in the control packet CP, for example the number of received packets (a *status of the PHY)*, number of transmitted data (a *status of the PHY)*, colliding packets (a *status of the PHY)*, CRC

error, over-sized packets (a *status of the PHY)*, under-sized packets (a *status of the PHY)*, packet settings (a *status of the PHY)*, packet parameters and/or specially defined packet particulars).

In regards to claims 8 and 19, *Chiang teaches circuitry to determine when to transmit the generated packets* (section 0021, the control packet is generated by the control packet generator when the MIB counters indicate at least one of the counted values of the management information data exceeds a threshold value).

Chiang and Raphaeli do not explicitly teach the circuitry is in PHY as in claim 8.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of circuitry being in PHY, as circuitry can be located in any component section based on system need, available space within the chip/board, cost and resource requirement to meet the need of a required form factor suggested by the standards; thus making the product compatible with available systems in the industry.

In regards to claims 9 and 20, Chiang teaches *a second component* (the second layer 74 in Figure 3), *the second component to identify packets generated by the PHY/Framer* (section 0035).

In regards to claims 10 and 21, Chiang teaches *a component* (Figure 3 and section 0035, the second layer 74 is equivalent to the driver 64) *to intercept the packets generated by the PHY* (section 0035).

In regards to claim 11, Chiang teaches *the second component comprises at least one of a framer, a device driver* (Figure 3 and section 0035, the second layer 74 is equivalent to the driver 64), *and a processor.*

In regards to claim 13, Chiang teaches *a framer* (Figure 2, section 0030, the control packet generator 6212 which generates control packet CP).

In regards to claim 14, Chiang teaches *input interface comprises an interface to a PHY* (Figure 2, physical layer device (PHY) 622).

In regards to claim 16, Chiang teaches *the data originating within the framer comprises at least one network interface statistic* (section 0030, depending on the types of objects, various management information data are included in the control packet CP, for example the number of received packets, number of transmitted data, colliding packets, CRC error, over-sized packets, under-sized packets, packet settings, packet parameters and/or specially defined packet particulars).

In regards to claim 17, Chiang teaches *at least one network interface statistic comprises at least one of: packets received, packets transmitted, bytes received, and bytes transmitted* (section 0030, depending on the types of objects, various management information data are included in the control packet CP, for example the number of received packets, number of transmitted data, colliding packets, CRC error, over-sized packets, under-sized packets, packet settings, packet parameters and/or specially defined packet particulars).

In regards to claim 22, Chiang teaches *the framer comprises at least one of: an Ethernet media access controller (MAC)* (Figure 2, MAC 621), *a High-Level Data Link (HDLC) framer, and a Synchronous Optical NETwork (SONET) framer.*

In regards to claim 23, Chiang teaches *a second input interface* (section 0035, the second layer 74 in Figure 3 which is equivalent to the driver 64 of FIG. 2) *to receive packets along a transmit path* (Figure 3, left arrows going downward); *a second output interface* (section 0035, the first layer 72 of the OSI model is equivalent to the network interface card 62 in the embodiment of FIG. 2); *and circuitry* (section 0035, the second layer 74 in Figure 3 which is equivalent to the driver 64 of FIG. 2) *to: identify packets in the transmit path destined for the framer* (Figure 2, MAC 621); *examine the contents of a packet destined for the framer, the contents identifying at least one of: at least one statistic to include in the generated packets, a request to generate at least one packet* (section 0035, query or polling), *at least one time to generate at least one of the generated packets* (section 0035, It is to be noted that only the control packet CP transmitted between the layer 72 or the network interface card 62 and the layer 74 or the driver 64 are transmitted according to the general packet transmission manner. For the transmission of the control packet CP from the layer 74 or the driver 64, it is conducted in response to the query or polling of the upper-level protocol layers 75 or the network communication protocol layer 65); *and transmit packets not destined for the framer* (data packets DP) *via the second output interface* (section 0035, the first layer 72 of the OSI model is equivalent to the network interface card 62 in the embodiment of FIG. 2) *to a component* (Figure 2, PHY 622) *further along a transmit path monotonically*

descending layers of a protocol stack (Figure 3, and section 0035, in a transmission procedure, the data packets DP asserted in the layer 74 is combined with the control packet CP and transmitted downwards).

In regards to claim 26, Chiang teaches *the set of at least one component comprises a PHY component* (Figure 2, PHY 822) *and a framer component* (Figure 2, Control Packet Generator 6212), *and wherein at least one of the PHY component and the framer component comprises the circuitry to generate packets in the receive path* (section 0030, when at least one of the management information data has a count exceeding a threshold value, the control packet generator 6212 generates a control packet CP).

In regards to claim 27, Chiang teaches *a network interface controller (NIC)* (FIG. 1, a network interface card 1 has a controller associated with it).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Raphaeli as applied to claim 1 above and further in view of Krishna et al. (US PAT 6094439, hereinafter Krishna).

In regards to claim 4, Chiang and Raphaeli teach a MAC component with PHY as described in the rejections of claim 1 above.

Chiang and Raphaeli do not explicitly teach output interface comprises a Media Independent Interface.

Krishna in the same field of endeavor teaches a special reconciliation layer, referred to as the multi-Media Independent Interface (m-MII), interfacing with the MAC (column 4 lines 1-16).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of a special reconciliation layer, referred to as the multi-Media Independent Interface (m-MII), interfacing with the MAC as suggested by Krishna. The motivation is that (as suggested by Krishna, column 4 lines 1-16) special reconciliation layer, referred to as the multi-Media Independent Interface (m-MII), which interfaces with the MAC, provides service functions required to efficiently and reliably distribute, multiplex, demultiplex, and aggregate traffic to and from physical layer (PHY) devices having transceivers.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Raphaeli as applied to claim 1 above and further in view of Rubino et al. (US PAT 6424629, hereinafter Rubino).

In regards to claim 6, Chiang teaches the data originating within the first component comprises at least one status of the PHY (section 0030, depending on the types of objects, various management information data are included in the control packet CP, for example the number of received packets, number of transmitted data, colliding packets, CRC error, over-sized packets, under-sized packets, packet settings, packet parameters and/or specially defined packet particulars).

Chiang does not explicitly teach the status having link up and link down info.

Rubino in the same field of endeavor teaches when the first protocol layer logic detects a logical channel failure that results in a logical connection failure, the first protocol layer logic triggers a routing table update by sending a signal (status) to the second protocol layer logic indicating that the logical connection failed. Likewise, when the first protocol layer logic determines that communication over the failed logical connection is restored, the first protocol layer logic triggers a routing table update by sending a signal (status) to the second protocol layer logic indicating that the logical connection is restored. The logical channel can be a physical communication channel (column 4 lines 44-53 and column 16 lines 9-10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of the status having link up and link down info as suggested by Rubino. The motivation is that (as suggested by Rubino, column 3 lines 10-12) this method allows a system to quickly and efficiently reconverge when the status of connection changes.

6. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Raphaeli as applied to claim 1 above and further in view of Eatherton (US PAT 6697382, hereinafter Eatherton).

In regards to claims 7 and 18 Chiang and Raphaeli teach a MAC component with

PHY and data originating within the MAC as described in the rejections of claim 1 above.

Chiang and Raphaeli do not explicitly teach the data comprises at least one of a sequence number and a timestamp.

Eatherton in the same field of endeavor teaches control packet comprises a timestamp (column 5 lines 20-32).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of control packet comprising a timestamp as suggested by Eatherton. The motivation is that (as suggested by Eatherton, column 1 lines 36-40) such method reliably and efficiently enables components to be synchronized; that is, each of the components reflect substantially the same time (within some small tolerance).

7. Claims 12 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Raphaeli as applied to claim 1 above and further in view of Bullman et al. (US PAT PUB 2003/0028658, hereinafter Bullman).

In regards to claim 12, Chiang and Raphaeli teach a MAC component with PHY as described in the rejections of claim 1 above.

Chiang and Raphaeli do not explicitly teach the PHY further comprises circuitry to intercept PHY configuration packets traveling along a transmit path monotonically descending the layers of the protocol stack.

Bullman in the same field of endeavor teaches PHY register read and write command packets are generated by the extended protocol layer and are intercepted (intercept circuitry) and parsed by the extended PHY device. The registers are any set of registers that are included in the extended PHY device to carry out any desired operations and services in the network. These registers may include conventional status registers such as the and/or any additional registers which are required due to modifications to standards (PHY configuration), introduction of new standards (PHY configuration), or for some other reason (Figure 2 and section 0024 and section 0022).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of circuitry to intercept PHY configuration packets traveling along a transmit path monotonically descending the layers of the protocol stack as suggested by Bullman. The motivation is that such method enables a system to reliably and efficiently configure the PHY via higher layer protocol; thus enable the system to communicate seamlessly with the network.

In regards to claim 24, Chiang teaches eliminating the control packets from their packet stream (Figure 3, shows Control Packet CP in the down arrow direction gets absorbed by element 72, first layer 72 of the OSI model is equivalent to the network interface card 62, and Data Packets CP continues to the network).

In regards to claim 24, Chiang and Raphaeli do not teach configure packet generation based on configuration packets received.

Bullman in the same field of endeavor teaches configure packet generation (Figure 2 and section 0024 and section 0022, modifications to standards, introduction of new standards) based on configuration packets (PHY register write command packets) received (Figure 2 and section 0024 and section 0022, PHY register read and write command packets are generated by the extended protocol layer and are intercepted and parsed by the extended PHY device. The registers are any set of registers that are included in the extended PHY device to carry out any desired operations and services in the network. These registers may include conventional status registers such as the and/or any additional registers which are required due to modifications to standards, introduction of new standards, or for some other reason).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of configure packet generation based on configuration packets received as suggested by Bullman. The motivation is that such method enables a system to reliably and efficiently configure the PHY and MAC via higher layer protocol; thus enable the system to communicate seamlessly with the network and it's own higher layer protocol.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiang and Raphaeli as applied to claim 1 above and further in view of System Packet Interface Level 4 (SPI-4) Phase 2 Revision 1: OC-192 System Interface for Physical and Link Layer Devices, hereinafter SPI-4 Phase 2.

In regards to claim 15, Chiang and Raphaeli teach a MAC component with PHY

as described in the rejections of claim 1 above.

Chiang and Raphaeli do not explicitly teach the using System Packet Interface (SPI) for output interface.

SPI-4 Phase 2, in the same field of endeavor teaches using System Packet Interface (SPI) for output interface from PHY (page 8 figure 5.1).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify Chiang and Raphaeli's system/method by incorporating the teaching of using System Packet Interface (SPI) for output interface from PHY as suggested by SPI-4 Phase 2. The motivation is that, (as suggested by SPI-4 Phase 2, page 8), SPI-4 has many advantages like Point-to-point connection (i.e., between single PHY and single Link Layer device), support for 256 ports (suitable for STS-1 granularity in SONET/SDH applications (192 ports) and Fast Ethernet granularity in Ethernet applications (100 ports)), in-band port address, start/end-of-packet indication, error-control code etc. Further motivation is that The motivation is that it is advantageous to adapt to known standards for implementation of SPI-4 Phase 2 based communication for following reason: Companies actively involved in adhering to standards more frequently reap short- and long-term cost-savings and competitive benefits than those that do not. Standardization can lead to lower transaction costs in the economy as a whole, as well as to savings for individual businesses. Standards have a positive effect on the buying power of companies. Standards can help businesses avoid dependence on a single supplier because the availability of standards opens up the market. The result is a broader choice for businesses and increased competition

among suppliers. Companies also have increased confidence in the quality and reliability of suppliers who use standards. In addition, standards are used by businesses to exert market pressure on companies further down the value chain, i.e., their clients. Thus, businesses can use standards to broaden their potential markets.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Salman Ahmed whose telephone number is (571) 272-8307. The examiner can normally be reached on 8:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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